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FPGA BASED HARDWARE LEVEL ANALYSIS OF INVERSE SINC FILTERS

P. K. Gaikwad

Department of Electronics, Willingdon College, Sangli, (M.S.), INDIA

pawangaikwad2003@yahoo.co.in

Abstract

This paper focuses on effect of cut-off frequency on the transition curve of the Inverse Sinc filter. The MATLAB Frequency Visualisation Tool, fvtool, was used to analyze the transition bandwidth variation in response to the change in cut off frequency of the digital filter. One of the imperative facilities provided in MATLAB software, to generate the Hardware Description Language (HDL) for the filter object i.e. '*generatehdl'* command, was used and the digital filter was hardwired in a reconfigurable device: Field Programmable Gate Array (FPGA). Using this MATLAB function the Soft Intellectual Proprietary (IP) Core was generated in Very High Speed Integrated Circuit Hardware Description Language (VHDL) and instantiated it in a top level module. For testing purpose of the filter at analogue front, using Digital Storage Oscilloscope (DSO), the Advanced RISC Machine (ARM) device was interfaced with the Xilinx FPGA Spartan 3E board: Nexys2. Every time the filter's cut off frequency was varied and new VHDL code was generated to implement in the FPGA and test it at the analogue front. The frequency response curves for such filters were analyzed at software as well as hardware levels. It was observed that, moving back to the cut off frequency from desired, there was a diversification from expected behaviour of the Inverse Sinc filter.

Keywords: ARM Microcontroller; FPGA; fvtool; Inverse Sinc; MATLAB

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