



# ASSESSMENT OF POWER OPTIMIZATION IN VLSI SYSTEM USING LAUNCH-OFF-SHIFT AND LAUNCH-OFF-CAPTURE TESTING

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## Abstract

The aim of testing of VLSI circuits is high-quality screening of the circuits by targeting performance-related faults. Though a compact check set with extremely effective patterns, every police work multiple delay faults is fascinating for lower check prices, such patterns increase shift activity throughout launch and capture operations. Sensible quality and value patterns could therefore find you violating peak-power constraints, leading to yield loss, whereas pattern with low shift activity constraints could cause loss in check quality and/or pattern count inflation. During this paper, a projected style for testability (DfT) support is conferred for sanctioning the utilization of a group of patterns optimized for value and quality and additionally in an exceedingly low power manner. 3 totally different DfT mechanisms are mentioned one for launch-off shift, one for launch-off capture, and one for mixed at-speed testing. The projected DfT support permits a style partitioning approach, wherever any given set of patterns, generated in an exceedingly power-unaware manner, may be utilized to check the planning regions one at a time, reducing each launch and capture power in an exceedingly design-flow compatible manner. Thus the check pattern count and quality of the optimized check set may be preserved, whereas lowering the launch/capture power

**Keywords-** Design partitioning, launch-off capture (LOC), launch-off shift (LOS), peak power reduction, test power reduction.

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## 1.INTRODUCTION

At-speed or perhaps faster-than-at-speed testing of VLSI circuits aims for a high-quality screening of VLSI circuits by targeting performance-related faults. Scan-based at speed testing necessitates load, launch, and capture operations for each take a look at pattern. Load operation is performed via scan/shift operations, filling up all the scan chains with the pattern. because the targeted defects area unit timing-related, these patterns ought to check whether or not transitions launched from scan cells will reach their destinations (scan cells) at intervals a useful clock amount. There are a unit principally 2 totally different schemes for launching transitions off the serially loaded pattern. within the launch-off-capture (LOC or broadside) take a look at[1], a practical capture operation launches transitions from the locations wherever the serially loaded pattern (V1) differs from the response of the combinative logic to V1, i.e., the launch pattern (V2). In launch-off-shift (LOS or skewed-load) take a look at[2], a single cycle shift operation launches transitions from the locations wherever the serially loaded pattern (V1) differs from its one-bit shifted version, i.e., the launch pattern (V2). In each scheme, a subsequent quick practical capture operation that is of a practical clock amount except the launch event sets a Dead line for the transitions to gain their destinations; a timing-related defect that slows down the chip below its rated clock speed is so exposed.

DfT-based strategies have received a lot of attention for dominant scan power throughout shifting or response capture[3],[4] However, several DfT-based ways square measure applicable solely to stuck-at fault testing[5],[6] and they can not be wont to cut back capture power within the launch cycle or capture cycle for broadside testing. Strategies that cut back capture power for broadside testing suffer from the downside of



inflated test-data volume [7], [8] or vital hardware overhead [9]. a brand new approach is thus required to cut back capture power for broadside testing, with minimum impact on test-data volume and hardware overhead. Yield loss issues area unit old in at-speed testing schemes [10], [11], Excessive switch activity throughout the launch cycle might end in elevated peak provide currents, resulting in IR drop that will increase the signal propagation delays within the combinatory logic.

The end result can't be differentiated from that of a timing-related defect, inflicting a useful chip to fail the at-speed check. Peak power throughout the launch cycle of at-speed testing ought to thus be reduced so as to avoid the yield loss evoked by IR drop. Vital analysis efforts are exhausted in reducing power dissipation throughout the launch and capture of at speed testing. Check pattern generation whereas accounting for the useful clock gating logic so as to supply patterns that disable components of the look throughout launch and capture has been projected in [12] and [13], to reduce peak power at the expense of pattern count inflation. Another approach that elevates pattern count whereas reducing peak launch power has been within the kind of generating patterns beneath the constraint that just one chain launches transitions whereas all chains capture them, [14]. Another similar scan-segmented resolution [15], partitions the scan cells into 3 regions wherever solely 2 out of 3 regions launch and capture any check pattern.

A partitioning approach has been projected in [16] wherever power wise pricey patterns square measure any analyzed via fault simulation to spot the situation of the care bits, that dictate the partitioning of the look throughout capture; with few problematic patterns, such associate degree approach will deliver power savings. X-fill approaches have additionally been projected [17], [18] wherever pattern count inflation is that the aspect result. Partitioning the look and testing one partition at a time has been projected to cut back launch and capture power in inherent self-test (BIST) [19], in LOS [20] and in LOC [21] testing schemes; all told these schemes, new generated patterns targeting one partition at a time find yourself loading the interface registers of different partitions further, acquisition take a look at time and information volume penalty. Similarly, pattern count increase has been seasoned even once the look is partitioned off via ILP that minimizes capture violations [22]; further take a look at patterns, probably of a high sequent depth, ought to be generated for the faults lost owing to capture violations. Finally, low-power automatic take a look at pattern generation (ATPG) solutions have additionally been projected [23].

## 2. SURVEY OF RELATED WORK

A new automatic take a look at pattern generation (ATPG) formula was introduced by Lee et al to search out the quantity of capture cycles (CCs) required to lower the height power.

Wen et al changed the ATPG engine specified it might generate take a look at patterns with reduced change activity throughout take a look at. rather than ever-changing however take a look at patterns square measure generated, Wen et al. centered on consciously filling the take a look at cubes to lower the change activity. All the previous works from this direction involve modifying the ATPG flows and aren't able to wear down the clock tree power, that has become the dominant contributor to the ability budget. In distinction, scan chain division may be a well-studied methodology for dominant scan power (including the clock tree power) throughout shift to wear down capture power reduction.

Rosinger et al. projected scan design with reciprocally exclusive scan segments for dividing the circuit. pantry man et al. projected to mix a power-aware ATPG rule with circuit partitioning to cut back take a look at power for at-speed take a look at. On the opposite hand.

Zhang et al. provided AN ATPG rule for locating take a look at patterns that might improve coverage exploitation bachelor's degree, once a circuit was divided into multiple scan segments. These mixed DFT/ATPG ways have emerged as a result of its not obvious the way to mechanically produce scan divisions that patterns may well be generated by the prevailing ATPG flows while not sacrificing the transition fault coverage.

Iwagaki et al. analyzed however bachelor's degree take a look at patterns may well be generated with partial scan. However, power isn't thought of in their analysis. To the most effective of our information, there are not any previous works that analyze however the utilization of partial scan affects the CUT once exploitation scan chain division to regulate take a look at power throughout at speed delay take a look at.



Bhunia et al. projected AN increased scan primarily based delay fault testing that reduces the world overhead in comparison to standard increased scan. However, the projected technique offers high space and delay overhead compared to LOC and LOS ways. Rather than exploitation an additional latch, a provide gating was projected to be used at the primary level of logic gates of a combinable circuit. A transition fault ATPG methodology flow for scan-based styles exploitation broadside (LOC) take a look at format is projected. Replicate and reduced circuits rework maps the cheat frame process of the transition fault ATPG to a single-time frame process on duplicated repetitious blocks with reduced connections.

Abadir and Zhu report high transition fault coverage exploitation this ATPG technique. A path-oriented take a look at generation procedure referred to as POTENT is projected in to come up with high-quality tests for transition faults. typical ATPG tools square measure unaware of the circuit states exercised throughout the useful operation of the circuit.

Zhen Chen et al Scan shift power is reduced by activating solely a set of scan cells in every shift cycle. In distinction to shift power reduction, the utilization of solely a set of scan cells to capture responses in a very cycle could cause capture violations, thereby resulting in fault coverage loss. So as to revive the initial fault coverage, new take a look at patterns should be generated, resulting in higher test-data volume.

Minimum violations partitioning, a scan-cell cluster technique that may support multiple capture cycles in delay testing while not increasing test-data volume. This technique relies on a number applied mathematics model and it will cluster the scan flip-flops into balanced components with minimum capture violations. Supported this approach, stratified partitioning is projected to create the partitioning technique routing-aware.

Ho Fai blow et at, Scan chain division has been with success accustomed management shift power by sanctioning reciprocally exclusive flip-flops at totally different times throughout the scan cycle. However, to regulate capture power while not losing transition fault coverage throughout at-speed scan take a look at, the prevailing automatic take a look at pattern generation (ATPG) flows ought to be changed. during this paper, we tend to gift a completely unique scan chain division rule that analyzes the signal dependencies and creates the circuit partitions specified each shift and capture power is reduced once exploitation the prevailing ATPG flows. This novel rule has been designed for the broadside take a look at application strategy, and a method for using partial scan once dividing the scan chains is additionally projected.

O. Sinanoglu et al, Shrinking feature sizes have increased deep sub-micron effects, leading to integrated circuits liable to timing-related defects. Rigorous take a look at quality necessities have thus mandated the utilization of at-speed testing schemes, however, excessive switch activity throughout the launch operation could lead to yield loss. style partitions technique that may cut back power dissipation throughout launch and capture operations within the launch-off-shift (LOS) primarily based at-speed testing theme. As against the prevailing partitioning techniques, the projected low-power framework permits the re-use of a (compact and high quality) set of patterns generated by a traditional power-unaware LOS ATPG tool as is, which might be applied in a very low power manner. To tackle this challenge, we tend to derive partitioning rules also because the non-intrusive DfT support required, sanctioning the transformation of power-thriftless patterns into power-frugal ones, whereas holding pattern count and take a look at quality (fault and supportive defect coverage) intact.

### **3. PROPOSED METHOD**

#### ***3.1 LOC TESTING***

To identify the planning regions, and therefore the scan cell teams properly, the s-graph of the planning may be partitioned off in to powerfully connected parts (SCCs) [24]. Associate SCC may be a cluster of nodes wherever every node within the SCC is accessible from the other within the SCC. It's secured that associate s-graph partitioned off into SCCs contains no cycles, delivering the acyclicity required. Multiple SCCs will kind an area.

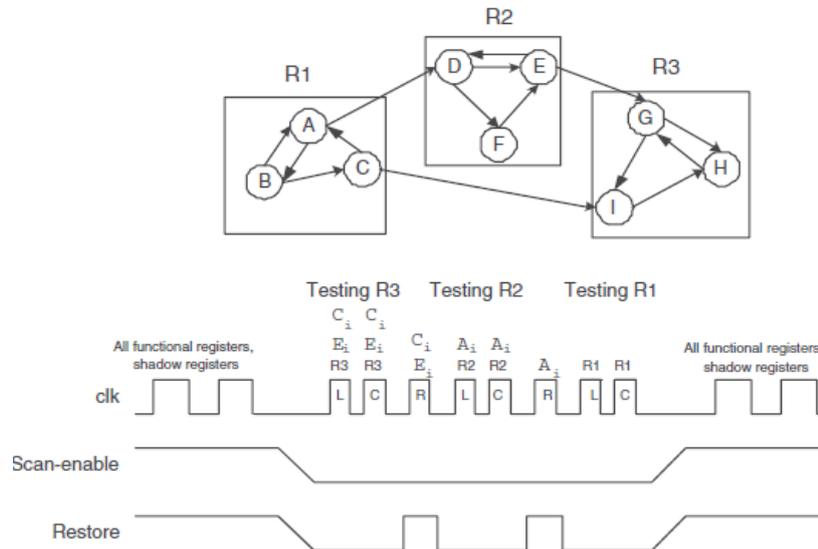


Figure.1.Example region interaction

Where region R1 (consisting of 3 SCCs) drives regions R2 and R3 (three SCCs each), and region R2 drives region R3. During this case, region R3 has to be tested first; launch and capture ought to even be performed within the registers of regions R1 and R2; but, just some of the registers in regions R1 and R2 ought to become involved, namely, the interface registers of R1 and R2. Interface registers of an {area |a district |a locality |a vicinity |a part |a section} are those who feed the registers of different regions through combinatory ways. Launching and capturing in exactly the interface registers of an area in testing another region permits a less expensive theme, as, this way, the load state restore capability would be required for less than the interface registers. During this example, upon the take a look at of region R3, the load state of solely the interface registers of regions R1 (some of the registers in C) and R2 (some of the registers in E) ought to be rehabilitated. With the load state of regions R1 and R2 rehabilitated, the take a look at of region R2 will proceed.

This time, launch and capture operations are performed not solely in region R2 however conjointly within the interface registers of R1 (some of the registers in A). After, the load state within the interface registers of R1 is rehabilitated, and therefore the take a look at of region R1 is conducted. A similar figure conjointly illustrates the temporal order diagram for the planned LOC testing theme

### 3.2 LOS TESTING

We illustrate the planned low-power LOS testing strategy in Fig. 2, wherever the eight SCCs shown square measure divided into 2 regions (A, B,C, D) and (E, F, G, H) throughout launch and capture operations. This time, a rewind signal is employed to form the interface registers shift within the reverse direction for one cycle, restoring their load state. Within the planned algorithmic program, we have a tendency to iteratively merge SCCs into larger regions. The top results of every merge operation is doubtless the elimination of a number of the interface registers, and so saving space value, and doubtless a rise in launch or capture power. In each step, the 2 regions, whose merge eliminates a most variety of interface registers, square measure merged; each step reduces the amount of regions by one, as a result.

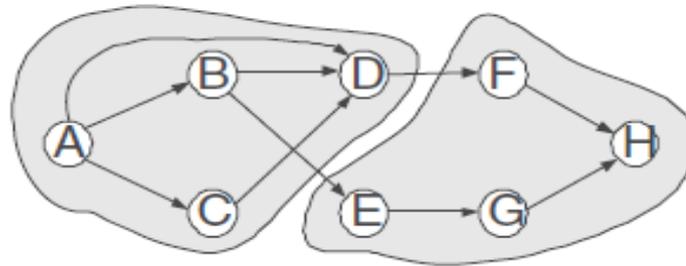


Figure.2. low-power LOS testing strategy

### 3.3 DfT OF LAUNCH-OFF-CAPTURE TESTING

To restore the load state (the bit shifted) of the interface (functional) register upon the launch and capture operations, one shadow (test) register is inserted for every interface register. Throughout the shift operations, the shadow register copies the content of the interface register, and through the capture window, the shadow register isn't clocked, guaranteeing that the derived worth within the last shift cycle is preserved. Upon each launch and capture operation that the interface register gets concerned in, its load state is reconditioned by repeating the content of the shadow register back to the interface register. Fig. three provides the DfT support for the load state restore mechanism. Effectively, an electronic device and a shadow flip-flop is inserted for the interface register, doubling the scale of the interface scan cell. The fresh inserted logic falls on the take a look at methods solely, acquisition to temporal arrangement penalty some. The restore signal is simply generated on-chip as shown within the same figure. The whole value is  $N_{int}$  MUXes and  $N_{int} + two$  flip-flops for  $N_{int}$  interface registers.

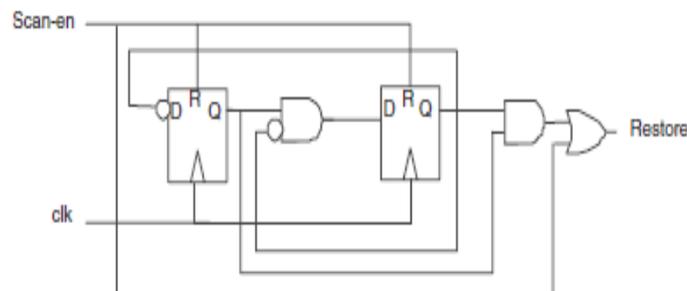


Figure.3.DfT support load states restore mechanism

### 3.4 DfT OF LAUNCH-OFF-SHIFTING TESTING

As the LOS theme launches transitions via a shift operation, a group of take a look at patterns is valid as long because the final scan cell ordering within the chain absolutely matches that in take a look at generation. Therefore, LOS pattern generation ought to be done behind scan sewing in standard LOS. The sole further constraint obligatory on scan sewing by the planned partitioning theme is that the interface registers of every region ought to be placed in consecutive positions on the scan chain which they have to be sewed during a bidirectional manner. Such a special sewing and therefore the associated DfT support square measure needed just for the interface registers so as to alter a correct rewind operation; step-down of the amount of interface registers helps to attenuate the realm value incurred.

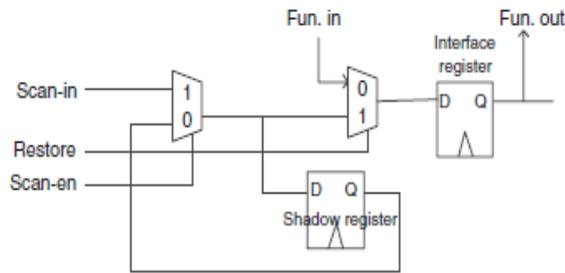


Fig.4. Restoration of Interface Register:

Finally, restoring the worth of the right little bit of a gaggle of interface registers behind the launch operation necessitates an additional flip-flop, that holds the worth of the right interface bit upon launch; a ulterior rewind operation restores the worth of the right interface register from the worth during this additional flip-flop. bidirectional sewing of the interface registers during a region needs one further electronic device for every interface register; this electronic device is inserted on the scan path (on the 1-input of the scan multiplexer), imposing no impact on the purposeful temporal arrangement of the look some.

The planned scan design that supports style partitioning into 2 regions (following the instance in Fig. 2) is provided in Fig. 4, conjointly illustrating the easy and efficient on-chip generation of the rewind signal out of the scan-enable and clock signals. The whole value is  $N_{int}$  MUXes and  $R_{int} + 1$  flip-flops for  $N_{int}$  interface registers and  $R_{int}$  regions that have a minimum of one interface register.

### 3.5 INTERFACE REGISTER TESTING

Because the LOS and LOC testing could unambiguously find faults during a reciprocally exclusive manner, a mixed take a look at with each LOS and LOC patterns generally yields a better fault coverage level compared to either testing theme applied alone. During this section, we have a tendency to define the DFT support needed to support low power mixed testing with each LOS and LOC patterns. Whereas the bidirectional sewing of interface registers fails to alter the planned low-power LOC testing, the shadow register support is utilized to alter the planned low power LOS testing; the shadow registers will replace the bidirectional sewing for the restoration of the load state in LOS testing.

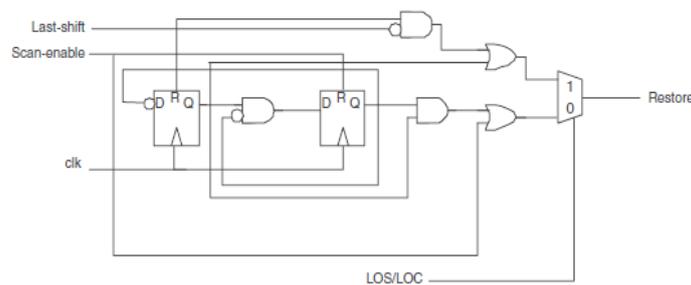


Figure.5.DfT for LOC/LOS Testing

Therefore, to support each low-power LOS and LOC testing, the design in Fig. three is utilized, however with a handful of changes; the shadow registers ought to be clocked solely throughout the shift cycles, and a unified Restore signal ought to be generated to support each LOS and LOC operations. The easy electronic equipment that generates this unified Restore signal is provided in Fig. 5. The LOS/LOC signal, that denotes the kind of take a look at for this pattern being applied and may be controlled by a programmable register bit (no want for a further pin), will build the choice of the correct signal.



#### 4. CONCLUSION

We planned DfT support which will restore the load state in interface registers in between the launch/capture operations within the style regions, enabling low-power LOC, LOS, and mixed at-speed testing. This way, a collection of patterns optimized for value and quality will be used as is, however in an exceedingly low power manner. During this methodology establish the fault detection and power improvement will be achieved.

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