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LOW POWER DSP ARCHITECTURE FOR WIRELESS SENSOR NODES USING DVFS ALGORITHM

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Abstract-The trend of smaller, portable and more capable electronic devices gives rise to a number of significant design and implementation problems of which the limited energy supply is the most determining factors. All these issues are jointly present in the field of Wireless Sensor Networks which is consequently a suitable context for research opportunities. Radio communication has highest energy consumption. To reduce the energy and power parallel prefix technique is used. This base paper describes the design and implementation of newly proposed folded tree architecture. Folded tree architecture has two phases. They are trunk and twig phase. The power is reduced to compare to the existing methods. For further performance improvement Dynamic Voltage Frequency Scaling concept introduced along with Digital Signal processor architecture. This paper is on a low-power real-time scheduler integrated into a common Linux is operating system. The low power schedule aims at reducing energy consumption in a system and uses Dynamic Voltage and Frequency Scaling to achieve its goal. The major advantage of Dynamic Voltage and Frequency Scaling is the output frequency, phase and amplitude can be precise and also rapidly manipulated under the control of a DSP. These combined characteristics have made this technology popular in military, radar and communication systems. The digital circuits used to implement signal processing functions do not suffer the effects of thermal drifts aging and component variations associated with their analog counterpart.

Key words—Digital processor, parallel prefix, wireless sensor network (WSN).

I. INTRODUCTION

Wireless sensor network (WSN) applications are medical field, environmental sensing, industrial inspection and military surveillance. Wireless sensor network node has three parts. They are sensors,

radio and micro controller. These three parts are combined with a limited power supply. Since radio transmissions are very expensive in terms of energy. The ratio of communication to computation energy cost range from 100 to 3000. So data communication must be traded for on the node processing which in turn can convert the many sensor readings into a few useful data values. The goal of this paper is to design low power WSN digital processor using parallel prefix technique. Radio communication exhibits the highest energy consumption in wireless sensor nodes has given their limited energy supply from batteries or scavenging, these nodes must trade data communications for on the node computation. Currently, it is designed around off the shelf low power microcontroller. The employing is a more appropriate processing element of the energy consumption can be significantly reduced. This paper describes the design and implementations of the newly proposed folded tree architecture for on the node data processing in wireless sensor networks are using parallel prefix operations and data locality in hardware. The Measurements of silicon implementation show an improvement of 10 –20× in terms of energy as compared to traditional modern microcontrollers found in sensor nodes.

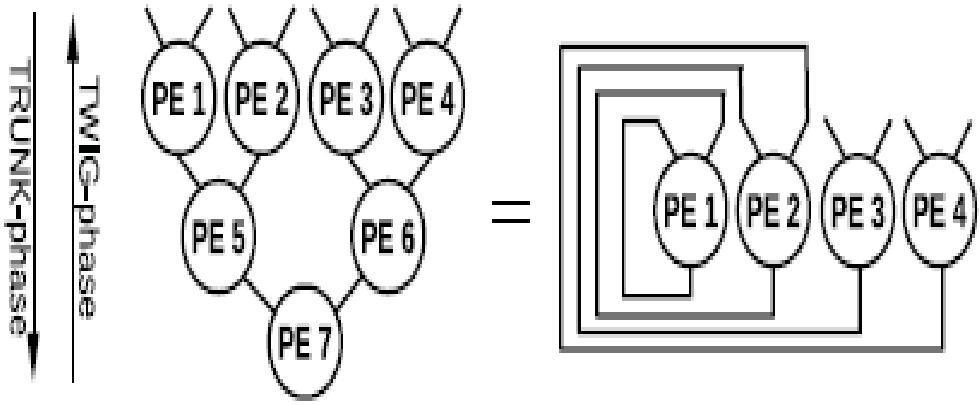
II. Related Requirements For Processing

Two key requirements are used to improve existing processing and control architectures can be identified.

Minimize Memory Access:

Modern micro controllers are based on the principles of divide and conquer strategy of ultra fast processors. In addition the lack of task specific operations leads to inefficient execution which results in longer algorithms and significant memory book keeping.

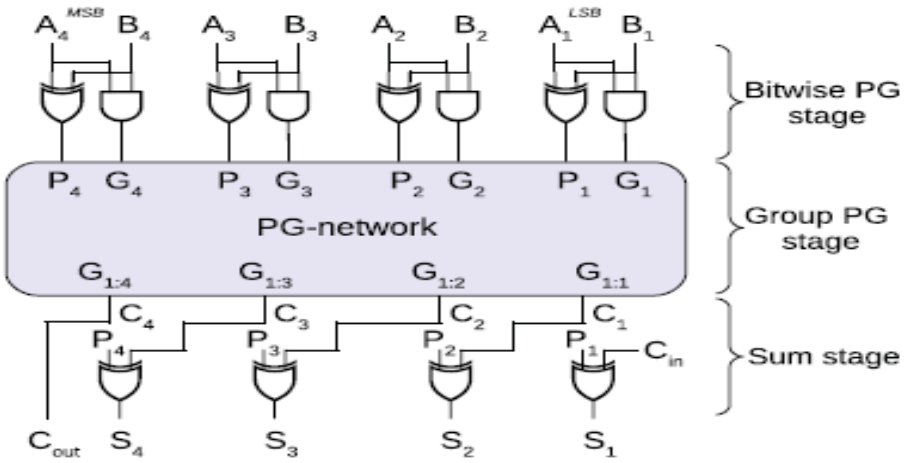
Combine Data and Control Flow Principles:



To manage the data stream and the instruction stream in the core functional unit has two exist approaches. Under control flow, the data stream is consequence of the data stream. The traditional processor architecture is a control flow machine with programs that execute sequentially as a stream of instructions. The data flow program identifies the data dependencies. The latter approach has been hugely successful in specialized high throughput application, such as multimedia and graphics processing. The characteristics of wireless sensor networks are Data driven, Many to few, Application specific.

III. Existing Method

In existing method binary tree is used. The disadvantages of this method is at a time only one node act as root nodes, other node act as leaves. So at a time only one data is send. Hence the power as well as energy is increased. Time requirement is high and interconnection is high. The proposed approach gives the limited power and energy. The time requirement is low as well as interconnection path is increased. So Folded tree architecture is proposed to send the data in the way of wireless communication technique.



Parallel prefix operations

In the digital design world, prefix operations are best known for their application in the class of carry look ahead adders. The addition of two inputs A and B in this case consists of three stages. A bitwise Propagate Generate(PG) logic stage, a group of logic stage, and a sum stage. The output of bitwise PG stage is given below.

Pi=Ai (xor) Bi , Gi = Ai . Bi
Group PG logic stage, which implements the following expression.
(Pi,Gi) (Pi+1,Gi+1) = (Pi.Pi+1, Gi+Pi.Gi+1)

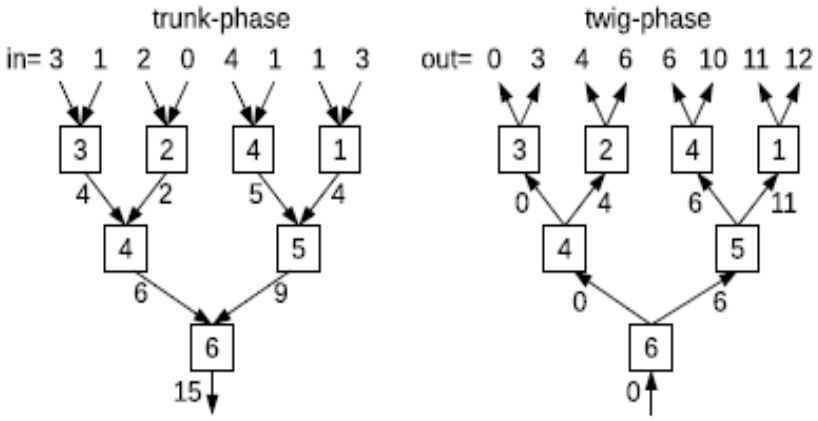
Consider the given example A= "1001" and B= "0101" are added together. The bitwise Propagate Generate logic of LSB first noted A={1001} and B={1010} returns the PG pairs for these values are(P,G)={(0,1);(0,0);(1,0);(1,0)}The carry array results are G = {1,0,0,0}.The sum results are S= {0,1,1,1}.The prefix element of the ordered set [3,1,2,0,4,1,1,3] is Σai=15. To calculate the prefix operations need two phases. They are Trunk phase and twig phase. In trunk phase the data is transmitted in the way of folded tree architecture. Twig phase is used to receive the data. The saved elements of trunk phase and twig phase are same. But the input of trunk phase and output of twig phase are different. The first two values of the input of trunk phase are denoted as left and right side value. Each left side value is saved, the saved element is called Lsave. Left side value only saved then it is added to the right side value. Again this value is saved to left side and The explanations of trunk and twig phases are given below

Trunk phase:

In the trunk phase the left value L is saved locally as L save and it is added to right value R, which is passed toward the root. It continues until the parallel prefix elements 15 are founds at the root. Note that each time, a store and calculate operation is executed.

Twig phase:

The twig phase starts, during which data moves in the opposite directions from the root to the leaves. Now the incoming values, beginning with the sum identity element 0 at the root is passed to the left childs, while it is also added to the previously saved L save and passed to the right childs. In the end, the reduced prefix set is the found at the leaves.



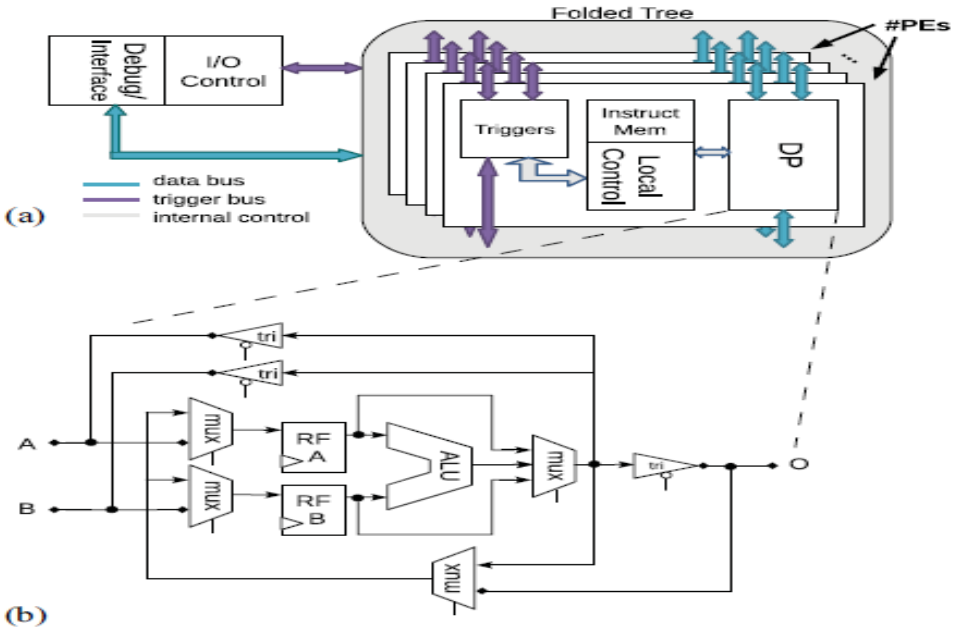
Folded tree:

To use folded tree architecture the area and power is reduced. The idea here is to fold the tree back onto the itself to maximally reuse the PE's. In doing so, P becomes the proportional to n/2 and the area is the cut in half. Note that also the interconnects are reduced. On the another hand, throughput decreases by a factor of log(n) but since the sample rate of different physical phenomena relevant for WSNs does not exceed 100 kHz, this leaves enough room for this trade off to be made.

IV. Proposed Approach

External low power algorithm DVFS(Dynamic Voltage Frequency Scaling) algorithm for further performance improvement. It continuously monitoring the processor utilisation with the DVFS algorithm adjust to the processor and consumes less power. It predict and applies the critical speed is the target frequency during the program's execution time. The algorithm relies on the prediction equation is constructed based on the correlation between the critical speed and the memory access rates. It is implemented the algorithm on the Android operating system. Our result shows that both the energy consumptions and the performance can be improves than the situation of simple selecting the lowest frequency.

DVFS is now usually supported by processors designed for mobile applications such as laptop computers or handheld devices in which multiple voltage and frequency levels can be utilised by the system software in different conditions to save on energy consumption. For example, when an application does not need to be run at the highest performance, it may reduce the frequency and voltage reduced the power consumption. Many DVFS researches have proposed methods to reduce power consumption for applications while trying to maintain their performance. However, the occasionally users to minimise the energy consumption.



V. Conclusion

In this paper presented the folded tree architecture of a digital signal processor for Wireless Sensor Nodes application. The design exploit the fact that many data processing algorithms for WSN applications can be described using parallel-prefix operations, introducing the much need flexibility. Energy is saved to the following: 1) limiting the data set by pre-processing with parallel-prefix operations; 2) the reuse of the binary tree as a folded tree; and 3) the combination of data flow and control flow elements to introduce a local distributes the memory, which removes the memory bottleneck while retains sufficient flexibility. The simplicity of the programmable PE's that constitute the folded tree network resulted in the high integrations, fast cycle times, and lower power consumption, Measurements of a 130 nm silicon implementation of the 16-bit folded tree with eight PEs were measured to confirm its performance. It consume down to 8 PJ /cycle. Compare to existing commercial solutions, this is at least 10× less in terms of overall energy and 2–3× faster.

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